CLAIM AMENDMENTS

The following is a complete listing of the pending claims:

Claims 1-20 (cancelled)

21. (Currently amended) A system for operating a GPS coarse acquisition (C/A) ~~C/A~~ code receiver comprising:

a plurality of channel means, each comprising:

means for forming x multibit digital segment values per C/A code period, x being an integer, each multibit digital segment value representing a sequential code segment of a received composite of satellite signals; and

a plurality of correlating means for correlating each multibit digital segment value with n satellite specific ~~set~~ sets of m different time delayed segments of C/A code, n and m being integers, to form at least n times m delay specific correlation values, wherein m is greater than the number of bits in each multibit digital segment value.

22. (Previously Presented) A system as in 21, further comprising a quadrature signal separator, the quadrature signal separator representing each digital segment value as a pair of quadrature signals.

23. (Previously Presented) A system as in Claim 22, further comprising:

a numerically controlled oscillator;

a multiplier;

a sine and cosine table accessed by the numerically controlled oscillator to provide rotational values for each pair of quadrature signals, the rotational values being multiplied with the quadrature signals in the multiplier and the product thereof being provided to the correlators for computing the correlation values.

24. (Previously Presented) A system as in Claim 21, wherein each pair of time delayed segments within each set of time delayed segments are separated from each other by a multiple of half-chip separations.

25. (Previously Presented) A system as in Claim 21, wherein each pair of time delayed segments within each set of time delayed segments are separated from each other by a multiple of quarter-chip separations.

26. (Previously Presented) A system as in Claim 21, wherein the number of bits in each multibit digital segment value is one or more times a value selected from the prime factors of then number of chips in a C/A code;

27. (Previously Presented) A system as in Claim 26, wherein the number of bits in each multibit digital segment value is 11.

28. (Previously Presented) A system as in Claim 21, wherein m is one or more times a value selected from the prime factors of then number of chips in a C/A code;

29. (Previously Presented) A system as in Claim 21, wherein m is greater than or equal to 22.

30. (Previously Presented) A system as in Claim 21, wherein n is one or more times a value selected from the prime factors of then number of chips in a C/A code;

31. (Previously Presented) A system as in Claim 21, wherein n is greater than or equal to 12.

32. (Previously Presented) A system as in Claim 21, wherein the product of m, n and the bits in each multibit digital segment value is one or more times the number of chips in a C/A code.